Enter please
Ebd Chang
2/22/06

IN THE CLAIMS:

Please amend claims 2, 6-10, 14, 15, 17, 18, 19, and 21-23 as follows.

1. (Canceled)

1 2. (Currently Amended) A transceiver circuit for transmitting and receiving data signals, said transceiver circuit comprising:

a transmitter subcircuit transmitting a pulse during a powered-down mode to indicate a status and using a first clock management mode, wherein said pulse differs from another pulse for indicating a power-on status;

a receiver subcircuit;

wherein said transmitter subcircuit and said receiver subcircuit each have its own power supply and means for activation and deactivation on the transceiver circuit; and

wherein when said transmitter subcircuit is in a power-on mode, the transmitter subcircuit transmits the another pulse for indicating the power-on status and uses a second clock management mode.

2 3. (Previously Presented) A transceiver circuit as recited in claim 1 2 wherein said pulse is a link pulse.

3 4. (Previously Presented) A transceiver circuit as recited in claim 1 2 wherein said pulse is a minimally powered pulse.

4 ~~5~~. (Previously Presented) A transceiver circuit as recited in claim ~~2~~ 1 wherein said pulse conforms to the another pulse for indicating the power-on status once a signal is received on said receiver subcircuit.

5 ~~6~~. (Currently Amended) A transceiver circuit as recited in claim ~~5~~ 4 wherein said transceiver enters into an auto-negotiation mode to identify the received signal on said receiver subcircuit.

6 ~~7~~. (Currently Amended) A transceiver circuit as recited in claim ~~2~~ 1 wherein said receiver subcircuit having a media independent interface for receiving the data signals, and wherein said media independent interface remains power-on during the powered-down mode and wherein said pulse is a normal link pulse.

7 ~~8~~. (Currently Amended) A transceiver circuit as recited in claim ~~7~~ 6 wherein said receiver subcircuit upon receiving an activity activates said transceiver into the power-on mode.

8 ~~9~~. (Currently Amended) A transceiver circuit as recited in claim ~~7~~ 6 wherein said transceiver in ~~a~~ the power-down mode powers-down all subcircuits except for said transmitter subcircuit and said media independent interface.

9 ~~10~~. (Currently Amended) A transceiver circuit for transmitting and receiving data signals, said transceiver circuit comprising:

a transmitter subcircuit transmitting a pulse during a powered-down mode to indicate a status and using a first clock management mode, wherein said pulse differs from another pulse for indicating a power-on status;

a receiver subcircuit having a media independent interface for receiving the data signals, said media independent interface remains power-on during the powered-down mode;

wherein said transmitter subcircuit and said receiver subcircuit each have its own power supply and means for activation and deactivation on the transceiver circuit; and

wherein when said transmitter subcircuit is in a power-on mode, the transmitter subcircuit transmits the another pulse for indicating the power-on status and uses a second clock management code.

10 ~~11~~. (Previously Presented) A transceiver circuit as recited in claim ~~10~~ 9 wherein said pulse is a link pulse.

11 ~~12~~. (Previously Presented) A transceiver circuit as recited in claim ~~10~~ 9 wherein said pulse is a minimally powered pulse.

12 ~~13~~. (Previously Presented) A transceiver circuit as recited in claim ~~10~~ 9 wherein said pulse conforms to the another pulse for indicating the power-on status once a signal is received on said receiver subcircuit.

13 ~~14~~. (Currently Amended) A transceiver circuit as recited in claim ~~13~~ 12, wherein said transceiver enters into an auto-negotiation mode to identify the received signal on said receiver subcircuit.

14 ~~15~~. (Currently Amended) A transceiver circuit as recited in claim ~~10~~ 9 wherein said receiver subcircuit upon receiving an activity activates said transceiver into the power-on mode.

15 ~~16~~. (Previously Presented) A transceiver circuit as recited in claim ~~10~~ 9 wherein said transceiver in the power-down mode powers-down all subcircuits except for said transmitter subcircuit and said media independent interface.

16 ~~17~~. (Currently Amended) A transceiver circuit for transmitting and receiving industry-standard data signals, said transceiver circuit comprising:

a transmitter subcircuit transmitting a minimally powered link pulse during a powered-down mode to indicate status using a clock management mode, wherein said minimally powered link pulse differs from pulse for indicating a power-on status; and

a receiver subcircuit having a media independent interface for receiving industry-standard data signals, said media independent interface remains power-on during the powered-down mode and the clock management mode, and upon receiving a signal activity activates said transceiver into a power-on mode;

wherein each of said transmitter subcircuit and said receiver subcircuit ~~each have~~ has its own power supply and means for activation and deactivation on the transceiver circuit; and

wherein when said transmitter subcircuit is in the power-on mode, the transmitter subcircuit transmits the another pulse for indicating the power-on status using another clock management mode.

17 ~~18~~. (Currently Amended) A transceiver circuit as recited in claim ~~17~~ 16 wherein said minimally powered link pulse conforms to the another pulse for indicating the power-on status once a signal is received on said receiver subcircuit.

18 ~~19~~. (Currently Amended) A transceiver circuit as recited in claim ~~17~~ 16 wherein said transceiver enters into an auto-negotiation mode to identify a received signal on said receiver subcircuit.

19 ~~20~~. (Previously Presented) A transceiver circuit as recited in claim ~~17~~ 16 wherein said transceiver in the power-down mode powers-down all subcircuits except for said transmitter subcircuit and said media independent interface.

20 ~~21~~. (Currently Amended) A transceiver circuit for transmitting and receiving data signals, said transceiver circuit comprising:

transmitter subcircuit means for transmitting a pulse during a powered-down mode to indicate a status and using a first clock management mode, wherein said pulse differs from another pulse for indicating a power-on status;

receiver subcircuit means for receiving the data signals;

wherein each of said transmitter subcircuit means and said receiver subcircuit means ~~each have~~ has its own power supply and means for activation and deactivation on the transceiver circuit; and

wherein when said transmitter subcircuit means ~~media~~ is in a power-on mode, the transmitter subcircuit means transmits the another pulse for indicating the power-on status and uses a second clock management mode.

21/ ~~22~~. (Currently Amended) A transceiver circuit for transmitting and receiving data signals, said transceiver circuit comprising:

transmitter subcircuit means for transmitting a pulse during a powered-down mode to indicate a status and using a first clock management mode, wherein said pulse differs from another pulse for indicating a power-on status;

receiver subcircuit means having a media independent interface for receiving the data signals, said media independent interface remains power-on during the powered-down mode;

wherein each of said transmitter subcircuit means and said receiver subcircuit means ~~each have~~ has its own power supply and means for activation and deactivation on the transceiver circuit; and

wherein when said transmitter subcircuit means is in a power-on mode, the transmitter subcircuit means transmits the another pulse for indicating the power-on status and uses a second clock management mode.

22 ~~23~~. (Currently Amended) A transceiver circuit for transmitting and receiving data signals, said transceiver circuit comprising:

a transmitter subcircuit means for transmitting a minimally powered link pulse during a powered-down mode to indicate a status and using a clock management mode, said minimally powered link pulse differs from another pulse for indicating a power-on status; and

a receiver subcircuit means having a media independent interface for receiving the data signals, said media independent interface remains power-on during the powered-down mode and uses the clock management mode, and upon receiving a signal activity activates said transceiver into a power-on mode;

wherein each of said transmitter subcircuit means and said receiver subcircuit means ~~each have~~ has its own power supply and means for activation and deactivation on the transceiver circuit; and

wherein when said transmitter subcircuit means is in the power-on mode, the transmitter subcircuit means transmits the another pulse for indicating the power-on status and uses another clock management mode.